REMARKS

In view of the above amendments and the following remarks, reconsideration of the rejections contained in the Office Action of June 12, 2003 is respectfully requested.

In order to make necessary editorial corrections, the entire specification and abstract have been reviewed and revised. As the revisions are quite extensive, the amendments to the specification and abstract have been incorporated into the attached substitute specification and abstract. No new matter has been added by the revisions. Entry of the substitute specification is thus respectfully requested.

The Examiner has rejected original claims 1-17 in view of the prior art. In particular, claims 1-8, 16, and 17 have been rejected as being anticipated by the Iijima reference (US Application 2001/0008309); and claims 9-15 have been rejected as being unpatentable over the Iijima reference in view of the Kawakami reference (US Application 2002/0027282). However, original claims 1-17 have now been cancelled and replaced with new claims 18-43, including new independent claims 18 and 32. For the reasons discussed below, it is respectfully submitted that the new claims are clearly patentable over the prior art of record.

New independent claim 18 is directed to a multi-layer board comprising a ceramic layer, a first resin layer over the first side of the ceramic layer, a third resin layer over the first layer, a polyimide film between the first resin layer and the third resin layer, and *a capacitor on the polyimide film*. As explained on page 4, lines 14-24 of the original specification, arranging a capacitor on a polyimide film located between a first resin layer and a third resin layer ensures that the capacitor will have an accurate capacitance and a low profile.

The Iijima reference discloses an interconnection substrate including a ceramic layer 201 and resin layers over the ceramic layer. Paragraph [0103] of the Iijima reference explains that the resin layers can be composed of a material such as photosensitive polyimide resin. However, as the Examiner has noted, the Iijima reference does not disclose components in the multi-layer board, such as a capacitor. Thus, the Iijima reference also does not disclose or suggest the arrangement of a capacitor on a polyimide film as recited in new claim 18.

The Kawakami reference discloses a composite monolithic electronic component, including layers 6, 7, and 8. As the Examiner has noted, paragraphs [0002] and [0006] of the Kawakami reference teach that the structure can accommodate elements such as a capacitor, an inductor, and/or a resistor. However, the Kawakami reference does not discuss the arrangement of any of these elements. In particular, the Kawakami reference does not disclose or suggest *a capacitor on a polyimide film*, as recited in new independent claim 18. Because there is no suggestion for this arrangement in the Iijima reference or the Kawakami reference, one of ordinary skill in the art would not be motivated to modify or combine the references so as to obtain the multi-layer board recited in new independent claim 18. Accordingly, it is respectfully submitted that new independent claim 18 and the claims that depend therefrom are clearly patentable over the prior art of record.

New independent claim 32 is directed to a multi-layer board comprising a ceramic layer, a patterned inductor on the ceramic layer, and a resin layer over a first side of the ceramic layer. A ground pattern is formed on the second side of the resin layer (i.e., the side of the resin layer not facing the ceramic layer), and the ground pattern and the patterned inductor are arranged so that no portion of the ground pattern is located on the second side of the resin layer opposite a portion of the first side of the resin layer that faces the patterned inductor. As explained on page 4, lines 5-8 of the original specification, the patterned inductor has an increased Q-factor due to this arrangement.

As the Examiner has noted, the Iijima reference does not describe components in the substrate, such as an inductor. Thus, the Iijima reference clearly does not describe the arrangement of an inductor in the multi-layer board as recited in claim 32.

The Kawakami reference suggests the presence of components, such as a capacitor or an inductor, but does not describe or suggest a patterned inductor and a ground pattern arranged so that no portion of the ground pattern is located on a second side of a resin layer opposite a portion of the first side of the resin layer facing the patterned inductor, as recited in new independent claim 32. Therefore, because the Iijima reference and the Kawakami reference do not, either alone or in combination, disclose or suggest the arrangement of the inductor with respect to the ground pattern as recited in claim 32, one of ordinary skill in the art would not be motivated to modify or combine the references so as to obtain the invention recited in new independent claim 32. Accordingly, it is

respectfully submitted that new independent claim 32 and the claims that depend therefrom are clearly patentable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

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MULTI-LAYER BOARD

FIELD OF THE INVENTION

[0001] The present invention relates to a multi-layer board used in small electronic equipment such as a portable telephone.

BACKGROUND OF THE INVENTION

[0002] As shown in Fig. 4, a conventional multi-layer board is formed with resin layers. For example, on a first surface 1, a pattern is formed, and an electronic component 2 is mounted. The electronic component 2 is connected to a second surface 4, third surface 5 or fourth surface 6 via a through hole 3 in order to be connected to a component such as an inductor formed on the surface 4, 5 or 6. Intervals between any of the first surface 1 through the fourth surface 6 are filled with a resin 7.

[0003] The conventional multi-layer board consisting of the resin layers, upon having the inductor formed thereon, shrinks with heat due to a temperature change, thus causing a characteristic such as an inductance to vary.

SUMMARY OF THE INVENTION

[0004] A multi-layer board has mechanical and electric characteristics stabilized against a temperature change. The multi-layer board includes a ceramic layer, a resin layer disposed over the ceramic layer, and a impedance element formed on the ceramic layer. The resin layer may have an electronic component mounted thereon.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Fig. 1 is a sectional view of a multi-layer board in accordance with a first exemplary embodiment of the present invention.

Fig. 2 is a perspective view of an essential part of the multi-layer board in accordance with the first embodiment.

Fig. 3 is a sectional view of a multi-layer board in accordance with a second exemplary embodiment of the present invention.

Fig. 4 is a sectional view of a conventional multi-layer board.

DETAILED DESCRIPTION OF THE INVENTION

(Exemplary Embodiment 1)

[0006] In Fig. 1, a ceramic layer 11 having a relative dielectric constant of about 10 (at 1MHz), has a top surface (a third surface) 11a provided with a resistor 12, inductor 13 and capacitor 14 formed thereon. The layer 11 has a bottom surface (a fourth surface) 25a provided with a resistor 15, inductor 16, and capacitor 17 formed thereon. These impedance elements, since being formed on both surfaces of the ceramic layer 11, are stable against an external temperature change.

[0007] A Resin layer 18 having a relative dielectric constant of about 4 (at 1MHz) has a top surface (a second surface) 18a provided with a pattern 19 formed thereon. The pattern 19 is electrically connected to the third surface 11a with an interstitial via-hole (hereinafter referred to as a hole) 20 and to a first surface 22a with a hole 21 to be connected to circuits. Since the relative dielectric constants of resin layers 18, 22 are lower than that of ceramic layer 11, a strip line formed on the second surface 18a can be wide, thereby having a reduced loss. This is preferable particularly in high frequency performance for improving a noise factor (NF).

[0008] The resin layer 22 having a relative dielectric constant of about 4 (at 1MHz) has a top surface (a first surface) 22a provided with a surface-mounted device (SMD) 23 and a bare chip device 24 mounted thereon.

[0009] The resin layer 25 has a relative dielectric constant of about 4 (at 1MHz) and a fifth surface 26a provided with a pattern 27 formed thereon. The pattern 27 is electrically connected to the fourth surface 25a by a hole 28 and to a sixth surface 26b of a resin layer 26 by a hole 29 to be connected to circuits. The hole 29 is a through-hole extending from the first surface

to the sixth surface 26b (from the top external surface to the bottom external surface of the multi-layer board).

[0010] Thus, the multi-layer board of the first embodiment has a six-surface structure, that is, includes the ceramic layer 11 as a core board, and the resin layers 18, 22, 25, and 26 over both surfaces of the layer 11. The resistors 12, 15 and inductors 13,16, since they are formed on the ceramic layer 11, have respective characteristics stabilized against any temperature change, thus having accurately-maintained values.

[0011] The first surface 22a, since it is provided with the SMD 23 and bare chip device 24 mounted thereon, contributes to an improved packaging-density, thus enabling the board to be small.

[0012] The resin layers 18, 22, 25, and 26, since they are stacked over both surfaces of the ceramic layer 11, 25, allow the multi-layer board not to warp and to be mounted on a base board of an apparatus without a gap.

[0013] In the case that the base board is a resin board, the multi-layer board can be mounted in close contact with the base board if the resin layer, of the multi-layer board, contacting the base board is made of resin having a thermal expansion coefficient close to that of the base board.

[0014] Fig. 2 is a perspective view of the impedance elements, the resistor 12, inductor 13, and capacitor 14 on the third surface 11a of the ceramic layer 11. The resistor 12 and inductor 13 are laser-trimmed, thus having a resistance and inductance adjusted accurately, and thereby having stable performance. In addition, the inductor 13 is formed on the ceramic layer 11 having a large relative dielectric constant, thereby having a large inductance despite its reduced size.

[0015] If a portion of the second surface 18a, corresponding to (opposite) inductor 13 is not provided with a ground pattern formed on the surface, the inductor 13 has an increased Q-factor.

[0016] The capacitors 14, 17 include electrode layers 14a, 14c, 17a, and 17c and dielectric layers 14b, 17b which are formed by printing and sintering. The dielectric layers 14b, 17b, upon being made of high dielectric material, provide the capacitors 14, 17 with large capacitances despite their reduced sizes.

(Exemplary Embodiment 2)

[0017] As illustrated with a sectional view of Fig. 3, a multi-layer board in accordance with a second exemplary embodiment includes eight surfaces. Instead of the fifth surface 26a of the board of the first embodiment, a fifth surface 30a facing a polyimide film 30 and a sixth surface 31a of the polyimide film and facing a resin layer 31 are inserted.

[0018] In Fig. 3, the sixth surface 31a of the polyimide film 30 is provided with a capacitor 32 formed by vapor deposition, so that the capacitor 32 has an accurate capacitance and a low profile.

[0019] Each multi-layer board of the first and second embodiments including the ceramic layer resists bending. Further, the multi-layer board is inexpensive since including the stacked resin layers, which are inexpensive.

ABSTRACT

A multi-layer board includes a ceramic layer and plural resin layers which are stacked together. The ceramic layer is provided with an impedance element formed thereon, and the uppermost resin layer is provided with an electronic component mounted thereon. The multi-layer board is stable against a temperature change.

MULTI-LAYER BOARD

Version with Markings to Show Changes Made

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DETAILED DESCRIPTION OF THE ~~PREFERRED EMBODIMENTS~~ INVENTION

(Exemplary Embodiment 1)

[0006] In Fig. 1, a ceramic layer 11 having a relative dielectric constant of about 10 (at 1MHz), has a top surface (a third surface) 11a provided with a resistor 12, inductor 13 and capacitor 14 formed thereon. The layer 11 has a bottom surface (a fourth surface) 25a provided with a resistor 15, inductor 16, and capacitor 17 formed thereon. These impedance elements, since being formed on both surfaces of the ceramic layer 11, are stable against an external temperature change.

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[0009] The resin ~~layers 25, 26 each having~~ layer 25 has a relative dielectric constant of about 4 (at 1MHz) ~~has~~ and a fifth surface 26a provided with a pattern 27 formed thereon. The pattern 27 is ~~conducted to a~~ electrically connected to the fourth surface 25a ~~with~~ by a hole 28 and to a sixth surface 26b ~~with~~ of a resin layer 26 by a hole 29 to be connected to circuits. The hole 29 is a

through-hole extending from the first surface 22a to the sixth surface 26b (from the top external surface to the bottom external surface of the multi-layer board).

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